Remarks:

Reconsideration of the application is requested.

Claims 1-11 and 16-20 are now in the application. Claims 19 and 20 have been added. Claims 2 and 16 have been amended.

In item 6 on page 2 of the Office action, claims 1-7 and 16-18 have been rejected as being obvious over Kuriyama (5,682,057) in view of Hatanaka (5,587,598) under 35 U.S.C. § 103. Applicant respectfully traverses.

Claim 1 defines a method for producing an electrical connection between integrated circuit chips, which comprises:

providing a first integrated circuit chip having a terminal and a signal terminal;

forming an electrically conductive connection between the terminal and the signal terminal of the first integrated circuit chip;

providing a protective structure that becomes conductive to dissipate electrostatic discharges;

providing a second integrated circuit chip having a terminal that is coupled to the protective structure;

disposing the first integrated circuit chip and the second integrated circuit chip adjacent one another;

electrically connecting the signal terminal of the first integrated circuit to the terminal of the second integrated circuit chip;

connecting the terminal of the first integrated circuit chip to a terminal of a package; and

subsequent to connecting the terminal of the first integrated circuit chip to the terminal of the package, severing the electrically conductive connection between the terminal and the signal terminal of the first integrated circuit chip using an energy pulse.

Kuriyama teaches providing a chip 3 with a transistor element 3a and a fuse element 7 in a common package 17 (see column 3, lines 6-11, 21-25, and 50-54). If the semiconductor chip 3 generates excessive heat due to an overcurrent or an excessive applied voltage, a narrow portion of a conductor strip 10 of the fuse element 7 is melt-cut so that external components connected into the load path are not damaged (see column 3, lines 55-67).

Kuriyama is not concerned with protecting the chip 3 from electrostatic discharges and does not teach or suggest anything in that regard. In the last two lines in the first paragraph on page 3 of the office action, the Examiner has stated that a protective structure is taught at column 5, lines 51-61, however this assertion is clearly incorrect. The cited passage merely describes the operation of the fuse element 7 to protect external components that are connected in the load path from damage.

Kuriyama does no teach or suggest:

providing a protective structure acting as a switch that becomes conductive when there is an overvoltage to dissipate an electrostatic discharge to a line for a supply voltage; and

electrically coupling at least the first terminal pad of the second integrated circuit chip to the protective structure.

The Examiner has also stated that it would have been obvious to form the protection structure taught by Hatanaka in the fuse formation method of Kuriyama (see the last three lines on page 3 of the office action). As will be discussed below, the two references teach fuses that have very different purposes and because of these differences, one of ordinary skill in the

art would not combine the references in the manner asserted by the Examiner.

The Examiner has cited column 4, line 61-column 5, line 4 of Hatanaka, however that passage merely describes the operation of the protective diodes 23, 24 after the fuse portion 11 is cut (See column 4, lines 38-44 and column 5, lines 5-7). Kuriyama teaches that after the chip 3 is excessively heated (because of an overcurrent or high applied voltage), the conductor strip 10 of the fuse element 7 is melt-cut by heat generated by the chip 3, and the chip 3 is disconnected so that the external components connected into the load path are not damaged (see column 3, lines 55-67).

Please note that, after the fuse element 7 of Kuriyama is cut, the packaged device 17 is no longer functional and there would be no need to protect the chip 3 from electrostatic discharges. In contrast to Kuriyama, Hatanaka teaches cutting a fuse to enable protective diodes to become functional.

In other words, if the teaching of Hatanaka regarding the protective diodes 23, 24, which are activated by cutting a fuse, were somehow incorporated into the fuse structure of Kuriyama as suggested by the Examiner, when the fuse is cut thereby enabling the incorporated protective diodes, the packaged device 17 of Kuriyama would no longer be functional

and there would be no need to protect the chip 3 from electrostatic discharges. One of ordinary shill in the art would not incorporate an electrostatic discharge device that becomes functional when the device to be protected becomes non-functional. There would have been no suggestion to combine the references.

With regard to claim 17, Kuriyama only teaches that when an overcurrent or an excessively high voltage is applied to the chip 3, the chip 3 radiates a temperature high enough to melt cut the narrow portion 10c of the conductor strip 10. There is no teaching or suggestion that the narrow portion 10c of the conductor strip 10 should be cut using a laser beam.

Claims 19-20 have been added to even further distinguish the invention. Support for claims 19 and 20 can be found by referring to the application at page 10, lines 19-22.

Kuriyama teach a temperature fuse element 7, which the Examiner has equated with the claimed first integrated circuit chip. There is no teaching or suggestion for the temperature fuse element 7 to include at least one transistor. The whole teaching clearly indicates that the only function of the temperature fuse element 7 is to disconnect the chip 3 from the external circuit when the chip 3 radiates a temperature high enough to melt cut the narrow portion 10c of the

conductor strip 10. A transistor is not necessary for this functionality. Therefore, claims 19 and 20 even further distinguish the claimed invention from the prior art.

Claim 2 has been amended to recite that the severing step is performed by intentionally applying an electrical current pulse to the terminal of the second integrated circuit chip. Claim 16 has been similarly amended. Support for the changes can be found by referring to the application at page 12, lines 8-11 and at page 13, lines 4-19. Additionally, it should be clear from the disclosure as a whole that the current pulse is intentionally applied in order to sever the constrictions.

In contrast, Kuriyama teaches that the conductor strip 10 is melt cut by heat generated from the application of an excessively high voltage or an overcurrent (column 3, lines 55-67). The melting of the conductor strip 10 acts to disconnect the chip 3 from external circuitry in order to protect the external circuitry from damage and to insure that only the chip 3 is damaged as a result of the excessively high voltage or overcurrent. Since this application of the excessively high voltage or overcurrent results in the packaged device 17 becoming nonfunctional, it should be clear that such a signal would not be intentionally applied. Therefore, claims 2 and 16 even further distinguish the claimed invention from the prior art.

In item 7 on page 5 of the Office action, claims 8-11 have been rejected as being obvious over Kuriyama (5,682,057) in view of Hatanaka (5,587,598) and further in view of applicant's prior art under 35 U.S.C. § 103. Applicant respectfully traverses.

Claim 8 includes:

providing a protective structure acting as a switch that becomes conductive when there is an overvoltage to dissipate an electrostatic discharge to a line for a supply voltage;

electrically coupling at least the first terminal pad of the second integrated circuit chip to the protective structure.

Claim 8 is patentable for the reasons specified above with regard to claim 1.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 8. Claims 1 and 8 are, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claims 1 or 8, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-11 and 16-20 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, he is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant

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